Instrumentation OpAmp

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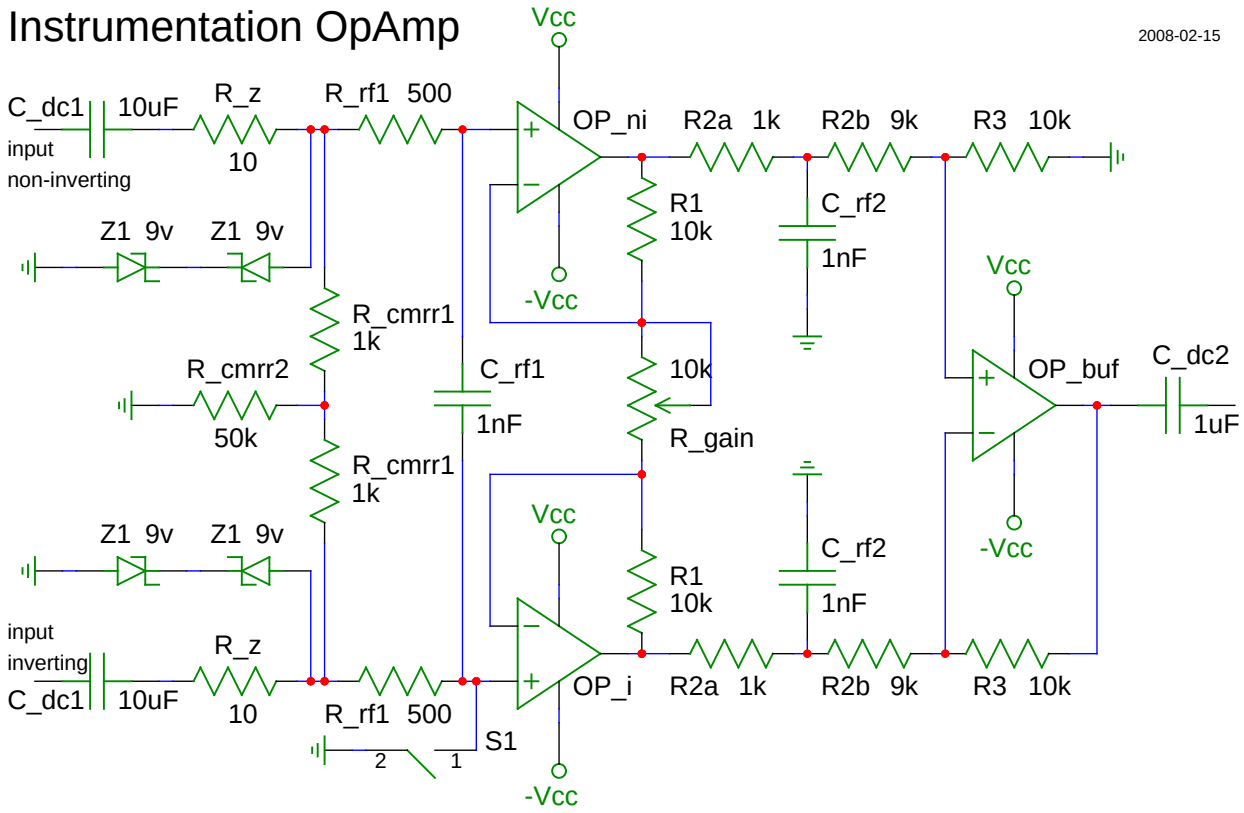

The 2 input buffers (OP_ni and OP_i) allow for simple gain and impedance matching to the differential amp.
If the impedance is imbalanced, CMRR will be much lower. Properly balanced, CMRR can be over 50db.
If R1=R2=R3: gain = 1 + 2R/R_gain. If R's are not equal: Vo/Vs = (1 + 2 * R1/R_gain) * (R3/R2).
The lowest possible gain is with R_gain infinite or removed (gain will be 1x). Smaller R_gain = larger output gain.
If R1=R2=R3, R_gain is usually value of R1 for a minimum gain of 3x total.
To enforce a maximum allowable gain, split R_gain into a static (usually 1/100 R1) and variable (R1) resistor in series.
Following this split of R_gain, the maximum output gain will be 201x. This is a good safety measure.
OP_buf is actually gain capable at the output stage. This gain (R3/R2) may be increased as needed.
R2 may be split (as shown) with a capacitor in the middle (C_rf2) to form a low pass filter to block RF noise.
R3 > R2 to keep OP_buf in amplifier mode. R2a+R2b may be adjusted accordingly.
R_rf1+C_rf1 forms a low pass filter to block RF noise in a floating ground configuration. freq=1/(2*PI*C*2R)
R_cmrr1+R_cmrr2 helps match cable impedance minor variations in a floating ground configuration (better CMRR).
R_cmrr1+R_cmrr2 also bleeds the offset that accumulates in C_dc1 pair. 100k to ground may also be needed for C_dc2.
C_dc1 is used to block DC on the input signal. This is typically from 1-47uF, with higher used for phantom power.
C_dc1 should be non-polar and rated for greater than 50v when used with phantom power.
R_z+Z1 forms a current limiting protection for Z1 and over voltage protection for inputs if the signal is too high or pops with phantom power. Zener diodes should be 1watt rated to handle sudden pops of phantom power.
An OpAmp may latch up if input signal exceeds power rails. Size the zeners to help prevent this. If input signal will be high and gain low, increase the zener voltage to help avoid non-linear distortion caused near the zener voltage.
C_dc2 is DC output block and is usually 1-10uF, but should not be needed if the input signal is already DC blocked.
Meter all the resistors carefully to match them as balance is very important in this configuration.
If the signal source is unbalanced, close switch S1 to short OP_i's input to ground.
Optional: input pad (static or variable) switch, input phase reversal switch, tone controls after output.
Capacitor Selection. Signal Path: polypropyline film for cleanest phase. Smaller (less than 1uF): use ceramic (NP0, C0G, XR7) for least ESR/ESL and fast high frequency response. Large: Electrolytics with low ESL.
For the Vcc voltage bypassing, see my Non-Inverting Op Amp General Design page.
Use metal foil or metal film resistors at 0.5-1 watt rating to keep noise down.
Op Amp Selection in order of preference: NOT TL07x, TL08x, and TL05x series. Basic: NE5532, NE5534. Preferred: OPA132/2132, OPA134/2134, OPA604/2604. A combined unit may be used to replace everything from OPNni to OP_i to OP_buf. Combined offers simpler and sometimes cheaper setups. Dual op-amps and combined units may suffer higher cross talk, though. Preferred: INA217, INA103 (low quality: INA121, INA126). See data sheet details for specs, wiring, and any extras that these chips may require.