Direct Drive Lead Acid Battery Desulfator (Type−3 "Jackhammer")

Original Design by Tusconshooter/Mark. Forum:
http://leadacidbatterydesulfation.yuku.com/topic/1162/Direct−Drive−Desulfator−Design?page=1

Brief Description. Most lead acid battery desulfators out there use a flyback design with inductors. While this does work, the inductor can only hold so much energy each pulse. If the battery has a high resistance, that energy won't be absorbed very well and will show up as a very high voltage spike on an oscilloscope. This spike may exceed the voltage ratings of various parts and cause damage.

The direct drive desulfators charge a capacitor bank to a known voltage and dump that energy into the battery as current. With a large capacitor bank, the dump can be very high energy. This allows for battery recovery to be much faster compared to flyback designs.

The overall design of this circuit is fairly basic on the conceptual level. AC wall power is rectified into DC. The large transformer feeds the capacitor banks, and the small transformer feeds the logic circuits. The charge MOSFET bank controls the charging of the capacitor bank and operates off an inverted signal to the discharge MOSFET bank ("charge" and "discharge" are never on at the same time). The discharge MOSFET bank essentially puts the capacitor bank in parallel with the battery for a very high current dump. The 555 logic circuits control the rate at which all this happens. With rapid repitition, the hard sulfate crystals eventually get broken down with minimal damage to the battery (as opposed to a constant higher voltage charge that used to be used in the past).

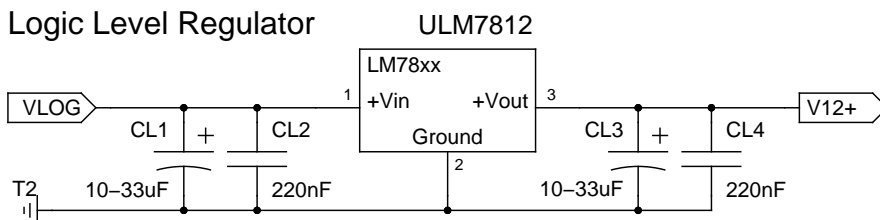This circuit version is fairly efficient and will generate very little heat if the parts are chosen correctly.
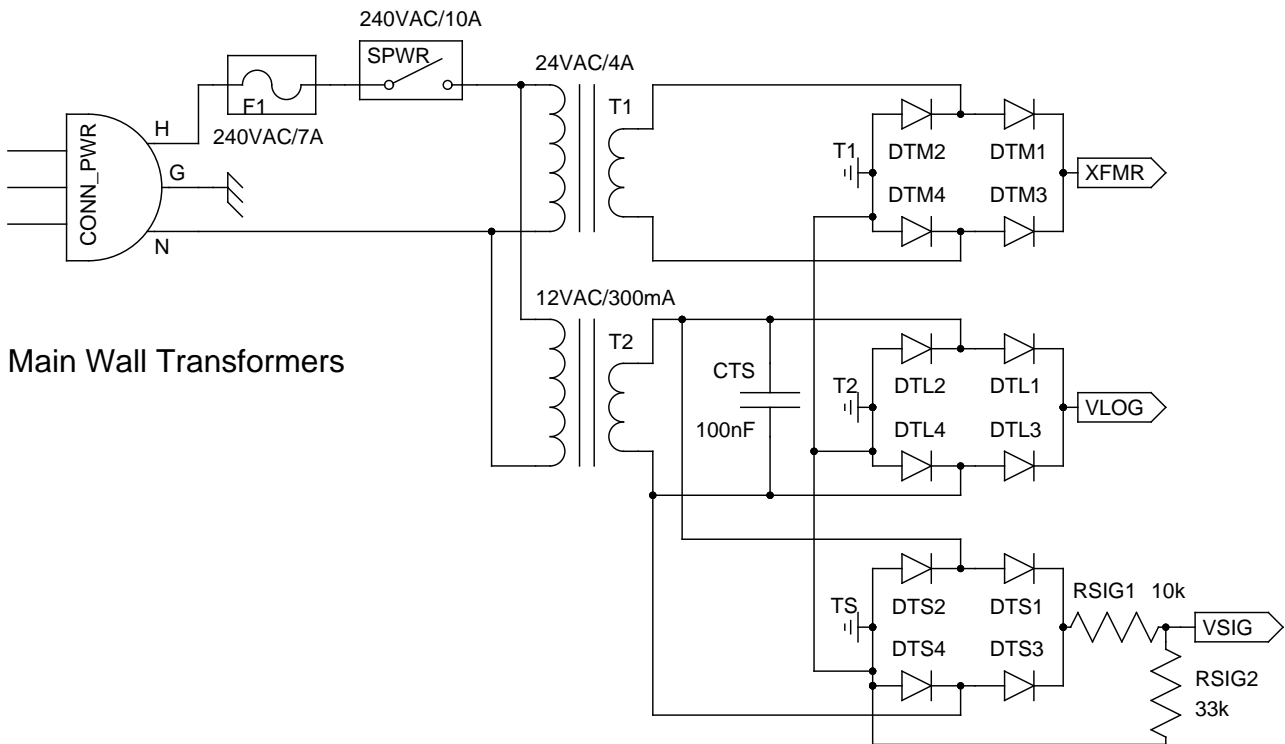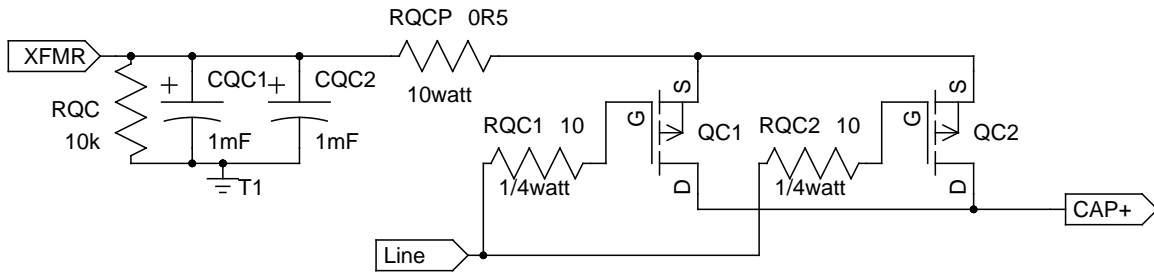

Main Wall Transformers

Use thick wires for the T1 transformer and diode bridge. T1 provides the high current power for the desulfator. T1's ampere rating will be the limiting factor of how much current will be pulsed into the battery. The fuse may be substituted with a circuit breaker. Diodes should be 10amp rated or better with high pulse current. T2 is a small transformer to provide power for the logic circuits. T2 will isolate the logic from the high ripple current, voltage drops, and ground bounces caused by the high current desulfator circuits.

VSIG provides a rectified AC wave form signal to the comparator used for Power Factor Correction (PFC). AC line frequency doesn't matter. Since this is a low current signal, standard rectifier or signal diodes may be used.
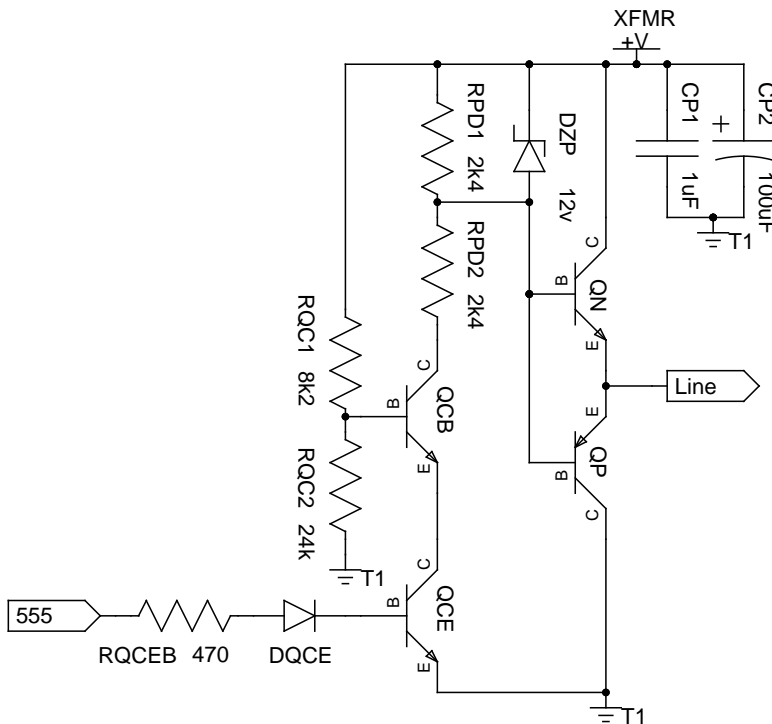
Logic Level Regulator   ULM7812

Charge MOSFET Bank: P–MOSFET Version

RQCP 0R5

XFMR

RQC
10k

CQC1 + CQC2

+

1mF   1mF

10watt

T1

RQC1 10

1/4watt

G

S

QC1

D

RQC2 10

1/4watt

G

S

QC2

D

Line

CAP+

Use thick wires connecting all the parts except the signal lines. RQC is a safety discharge resistor to drain the capacitors when the power is turned off. RQCP is used to take the edge off the initial surge current for parts safety and longevity. Both MOSFET's and capacitors have a limit on the current they can instantly handle. If the MOSFET's get hot, RQCP may be slightly increased (and/or charge pulse lengthened). Use low ESR capacitors for the electrolytics. Higher values are acceptable. For safety and longevity, capacitor voltage rating should be at least 50% above the rectified transformer voltage. Since the charging time is much longer compared to the discharging time, fewer P–MOSFET's are needed compared to the discharge N–MOSFET bank. Duplicate RQC+QC blocks for higher output. Choose P–MOSFET's based on the discharge N–MOSFET bank criteria (although these don't have to have as high of ratings). A low resistance MOSFET shouldn't get hot, but add a small heat sink with a little thermal compound to it anyways.

P–MOSFET Non–Inverting Level Shifted Cascode Line Driver

XFMR
+V

RPD1 2k4

RPD2 2k4

DZP
12v

CP1

+

1uF

CP2
100uF

T1

RQC1 8k2

RQC2 24k

QCB

C

B

E

QN

C

B

E

E

B

QP

C

Line

T1

555

RQCEB 470   DQCE

QCE

C

B

E

T1

P–MOSFET gates have a limited voltage range before they are blown. Since the XFMR voltage is higher, the gate voltage has to be level shifted with a limit. DZP offers this protection.
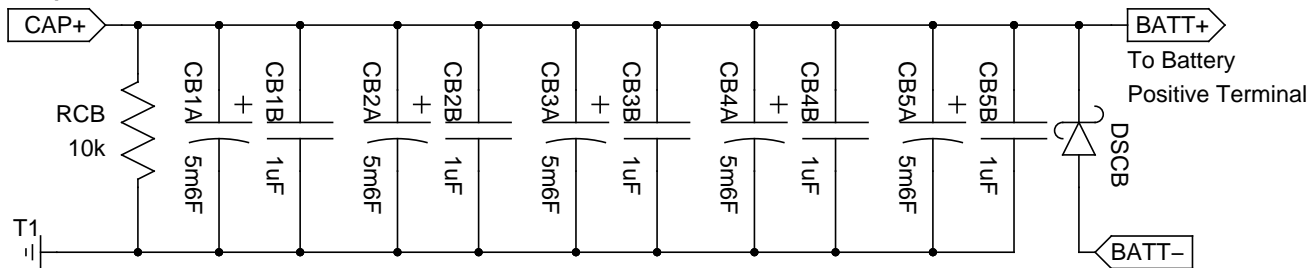
While this is technically a non–inverting line driver, the Line output is inverted relative to the 555 input as P–MOSFETs take an inverted signal. Remember that a P–MOSFET gate goes negative relative to the source to turn it on.

QN becomes an NPN high side switch and won't saturate once the emitter charges. QP is used to pull the line down to ground potential.

DZP needs to be about 3v less than the maximum MOSFET gate voltage to account for 3x diode drops of the transistors.
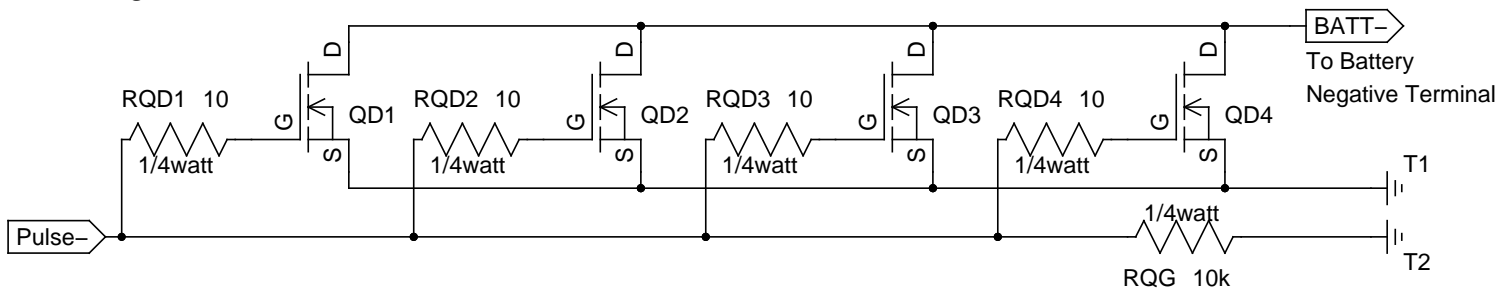
These parts need to be rated for the full XFMR voltage range.

Capacitor Bank

CAP+ ⟩

RCB
10k

CB1A 5m6F   CB1B + 1uF   CB2A 5m6F   CB2B + 1uF   CB3A 5m6F   CB3B + 1uF   CB4A 5m6F   CB4B + 1uF   CB5A 5m6F   CB5B + 1uF

DSCB

⟨ BATT+ ⟩
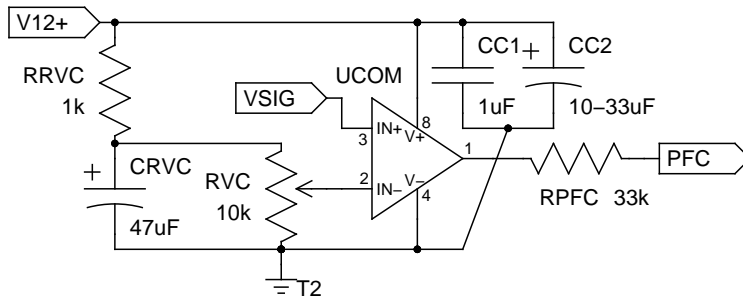To Battery
Positive Terminal

T1

⟨ BATT− ⟩

Low ESR capacitors connected to very thick wire. Using larger and more capacitors is acceptable. Total capacitance
should be around 20−30mF. For safety and longevity, capacitor voltage rating should be at least 30% above the
rectified transformer voltage. RCB is a safety discharge resistor to drain the capacitor bank when the power is off.
DSCB helps protect against inductive ringing damage. It should be high speed and high pulse current rated for
over 100 amps. An MBR10T100 would be a good choice.

Discharge MOSFET Bank

BATT− ⟩
To Battery
Negative Terminal

RQD1 10   QD1   RQD2 10   QD2   RQD3 10   QD3   RQD4 10   QD4

1/4watt   1/4watt   1/4watt   1/4watt

T1

1/4watt

Pulse− ⟩

RQG 10k

T2

Duplicate RQ+Q blocks for higher output. Use very thick wire for drain and source connections. RQG is a safety pull
down resistor to make sure the N−MOSFET gates do not float. Choose MOSFET's based on 70−100V, 80−150 amps,
300−500 peek amps, fast rise and fall times (less than 130nS, less than 50nS ideal), and low resistance (less than
0.005ohm). Preferred choices: IRFB3307 or IRFB4710 (mine are NXP PSMN6R5−80PS). A low resistance MOSFET
shouldn't get hot, but add a small heat sink to it anyways.

PFC Comparator

V12+ RRVC 1k UCOM CC1 + CC2 VSIG 1uF 10–33uF IN+ V+ 8 1 PFC + CRVC RVC 10k 2 IN– V– 4 RPFC 33k 47uF T2 3

Choose a comparator model that uses a pull up resistor on the output (but don't actually implement the pull up resistor). When the comparator's output is high, the output pin will be high impedance and not interfere with anything. When the comparator's output is low, it would short one of the signal lines to ground and stop the 555.
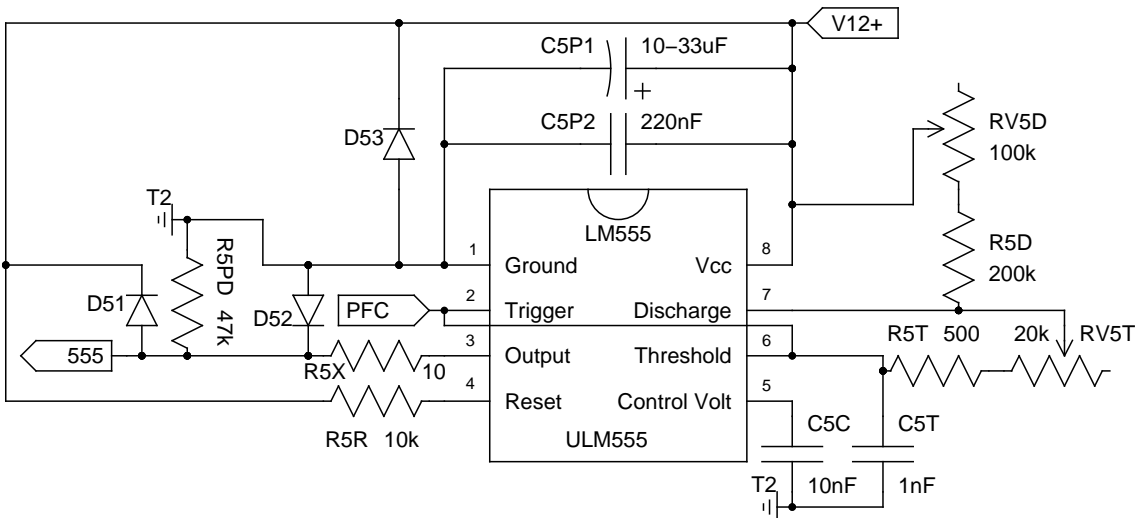
RPFC shouldn't be higher than 50k. The scope'd output shows a DC rise that gets too high at around 50k. 10k should be considered the minimum value. Resistor values too low may stress the 555 chip.

Generally speaking, RVC should be set to about half value for most cases.

The idea is to leave the capacitor bank charged during the wait time instead of fully dumping the capacitor bank into the battery and having a really high recharge current after the wait time ends. Looking at this backwards, after the wait time ends, the capacitor bank will probably be charged a little higher than usual and give a higher pulse current the first time. Since the PFC sub–circuit would cause regular wait periods and allow a little extra cool down time, perhaps the desulfator output could be boosted a little more to compensate.

I use a salvaged LM393 chip for my comparator. For multiple comparators in one chip, read the data sheet for how to disable the extra comparators so they don't oscillate and throw noise into the line.

Frequency Circuit

V12+ C5P1 10–33uF + C5P2 220nF RV5D 100k D53 R5D 200k T2 R5PD 47k LM555 1 Ground Vcc 8 D51 D52 PFC 2 Trigger Discharge 7 R5T 500 20k RV5T 555 R5X 10 3 Output Threshold 6 R5R 10k 4 Reset Control Volt 5 C5C C5T ULM555 T2 10nF 1nF
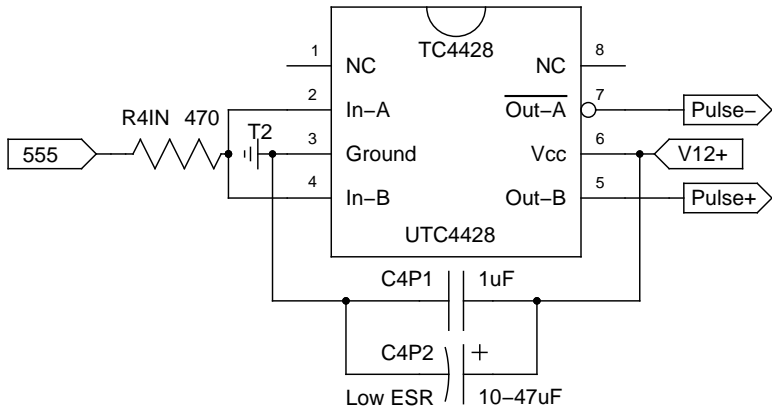
CLEAN OFF EXCESS FLUX!!! Resistors made by left over flux will cause the 555 to lock up.

All 3 brands of my 555's had a +3v spike on the top of the square wave and –3v spike below ground. This was somewhat minimized after the output was hooked to a load. D51, D52, and D53 are 1n4148's to help protect agains that. Running the 555 unloaded is not recommended. I've blown a few of my 555's, so the enhanced and protected version as shown is recommended. R5PD is a small pull down resistor to make sure the output line doesn't float and will sink weak coupled noise that makes it way onto the wire. R5X is a small output resistor to help limit initial current surges. It shouldn't be too big as steep slope square waves are needed on the MOSFET drivers. Note that the maximum 555 output is 200mA. I recommend using a DIP8 socket for all the chips since it's much easier to replace blown chips.
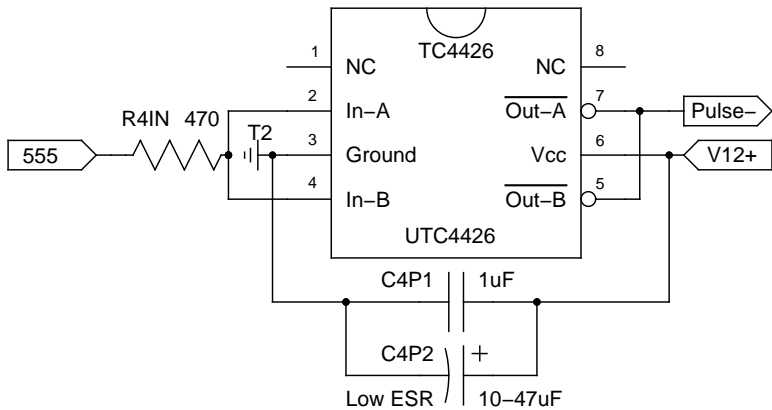
Scope'd from the MOSFET gate, the 555 should be delivering a 1–3uS pulse and a 200–300uS space. When setting up the 555, try to keep the duty cycle below 1% or things will deliver too much current, over heat, and burn out. The low duty cycle also allows time for the capacitor bank to properly recharge. Mine runs with these settings at about 3kHz. RV5D will increase the space as resistance increases (pulse width doesn't change). RV5T will make the total pulse cycle longer as resistance is increased (both pulse and space are changed). R5D+RV5D should start around 300k. R5T+RV5T should be about 1k. Note that for 555 calculations, RV5D+R5D are RA, RV5T+R5T are RB, C5T is C1, and C2 is the Control Voltage stabilizer (also a typicall 555 has a 100nS rise and fall time). Even with these minimal settings, the battery charge may float well above 14v. Keep an eye on it and be careful.

Note that for testing the full desulfator, pull out the frequency chips (555 and comparator) and the line driver chips (TC4426) and use a wire to manually run through all the charge and discharge stages to make sure they operate properly.
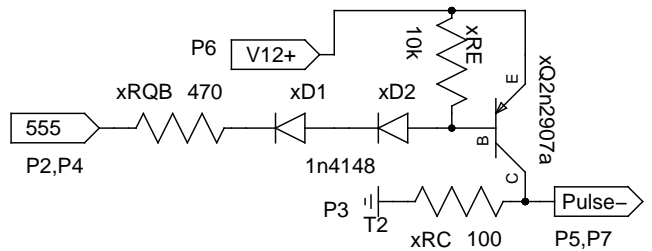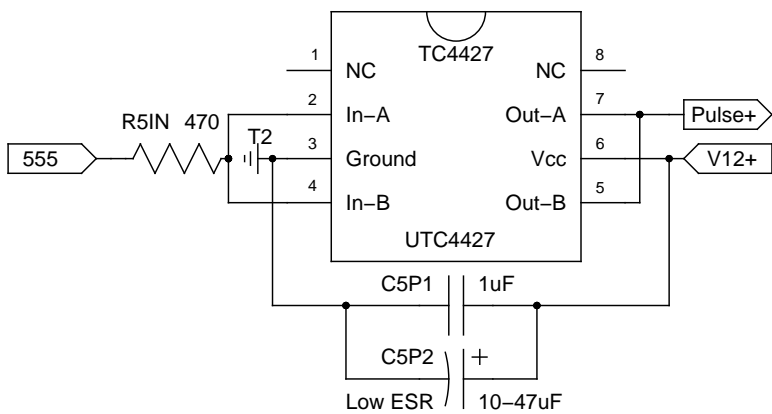
Inverting And Non–Inverting MOSFET Driver

TC4428

1	NC	NC	8
2	In–A	$\overline{\text{Out–A}}$	7
3	Ground	Vcc	6
4	In–B	Out–B	5

UTC4428

555 — R4IN 470 — T2

Out–A 7 → Pulse–
Vcc 6 → V12+
Out–B 5 → Pulse+

C4P1 1uF

C4P2 + Low ESR 10–47uF

Inverting MOSFET Driver (Preferred Chip For This Project)

TC4426

1	NC	NC	8
2	In–A	$\overline{\text{Out–A}}$	7
3	Ground	Vcc	6
4	In–B	$\overline{\text{Out–B}}$	5

UTC4426

555 — R4IN 470 — T2

$\overline{\text{Out–A}}$ 7 → Pulse–
Vcc 6 → V12+

C4P1 1uF

C4P2 + Low ESR 10–47uF

–––old inverting MOSFET driver–––

P6 V12+

10k xRE

xRQB 470   xD1   xD2   xQ2n2907a

555
P2,P4   1n4148

P3 T2   xRC 100   Pulse–
                    P5,P7

Non–Inverting MOSFET Driver

TC4427

1	NC	NC	8
2	In–A	Out–A	7
3	Ground	Vcc	6
4	In–B	Out–B	5

UTC4427

555 — R5IN 470 — T2

Out–A 7 → Pulse+
Vcc 6 → V12+

C5P1 1uF

C5P2 + Low ESR 10–47uF

–––old non–inverting MOSFET low side driver–––

P5,P7 Load

xD1   xD2   xQ2n2222a

555
P2,P4   xRB1 470   1n4148

P3 = T2
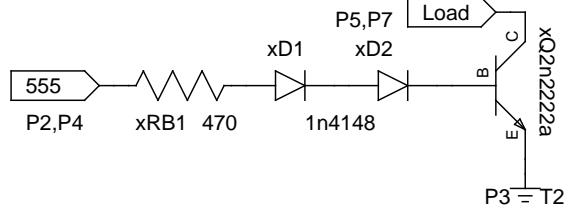
Inverting and non–inverting MOSFET drivers. If the DIP8 chips cannot be found, use the discrete transistor circuits to the right (pin numbers are given to plug into the DIP8 sockets). The TC4428 contains both on one chip. It cannot output as much current as both channels tied together, but that's probably not a problem in most instances.

Failed Charge N–MOSFET Bank
(left in for historical reasons)

DTDR

V2X   RTDR1 10k   QTDR   C B E   V2XR
DTDR
CTDR1 (100uF   CTDR2 1uF
DZTDR 12v
XFMR   RTDR2 5k6   TD

100uF   CTD1   DTD2
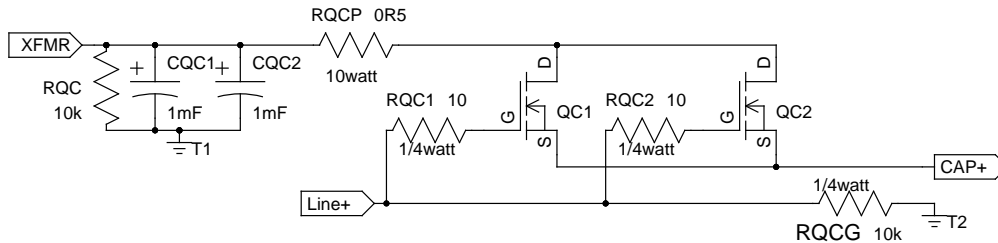DTD1   CTD2 100uF   RTD 47k   V2X
T1
T1   DTD3   TD
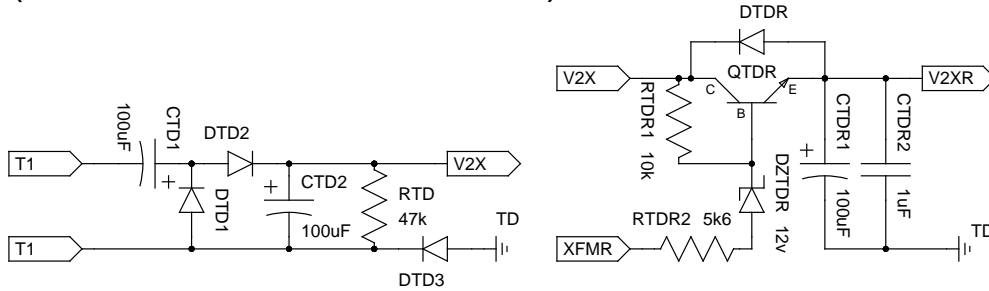
At this time, none of the doubler and driver circuits work as expected and should NOT be used.
These are left in for historical and learning reasons.

Voltage doubler circuit only required if the Charge MOSFET Bank is made of N Channel MOSFETs.
N–MOSFETs require +10–20volts over their source pins to properly drive their gates to full open in this configuration.
Note that some N–MOSFET gate ratings are only 15volts. 12volts is a good compromise.
CTD1 needs to be rated 1x the rectified voltage from the transformer and CTD2 is 2x. Anything from V2X to TD ground should be rated for 2x.
Considering periodic instabilities of doublers, higher voltage parts are a good choice for safety.
A Greinacher Doubler should be used as shown. A Delon Bridge Doubler will feed voltage back into XFMR and will raise it too high.
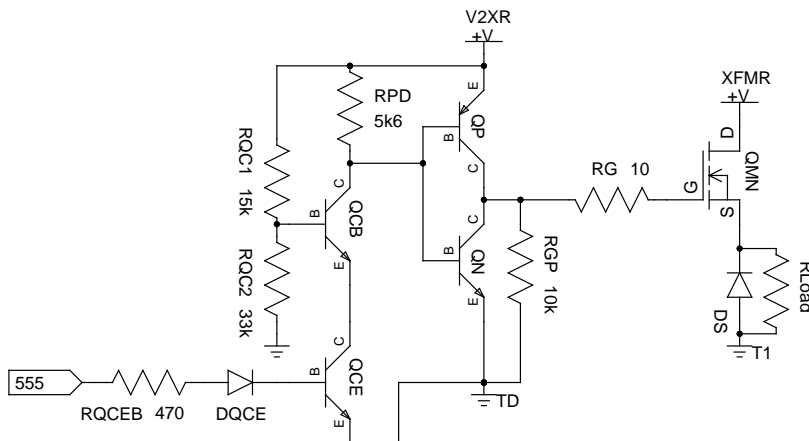
The *TDR* parts form a simple voltage regulator sitting on top of the XFMR voltage. All these parts need to be rated for 1x the XFMR
voltage except CTDR2 which should be 2x. Note that the ground of TZDTR does not connect to the TD ground.
Considering periodic instabilities of doublers, higher voltage parts are a good choice for safety.
V2XR should be about 12v above XFMR. QTDR needs to be at least 1amp rated.
It will get warm but should not get overly hot since all it's driving are the N–MOSFET gates.

Charge MOSFET Bank: N–MOSFET Version

RQCP 0R5

XFMR
RQC 10k   CQC1 1mF   CQC2 1mF   T1
10watt
RQC1 10   QC1   RQC2 10   QC2
1/4watt   1/4watt   CAP+
Line+
1/4watt
RQCG 10k   T2

Use thick wires connecting all the parts except the Pulse+ lines. RQCP is used to take the edge off the initial surge
current for parts safety and longevity. Both MOSFET's and capacitors have a limit on the current they can instantly
handle. If the MOSFET's get hot, RQCP may be slightly increased (and/or charge pulse lengthened). Use low ESR
capacitors for the electrolytics. Higher values are acceptable. For safety and longevity, capacitor voltage rating
should be at least 50% above the rectified transformer voltage. Since the charging time is much longer compared
to the discharging time, fewer MOSFET's are needed compared to the discharge MOSFET bank. Duplicate RQC+QC
blocks for higher output. Choose MOSFET's based on the discharge MOSFET bank criteria (although these don't
have to have as high of ratings). A low resistance MOSFET shouldn't get hot, but add a small heat sink with a little
thermal compound to it anyways.

Proposed High Side N–MOSFET Cascode Line Driver

V2XR +V
RQC1 15k   RPD 5k6   QP   XFMR +V
RQC2 33k   QCB   QN   RG 10   QMN
RGP 10k   RLoad
555   RQCEB 470   DQCE   QCE   DS   T1
TD

Note that this one assumes V2XR is +12v regulated over XFMR.